## REMARKS

Claims 2-7, 9-10, 12-13 and 15-20 are currently pending in this application, as amended. Claims 1, 8, 11, 14 and 21 have been canceled. **Claims** 2, 5-6, 9, 15, 17 and 20 have been amended to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Claim 5 has been rewritten in independent form and has been amended to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Claims 6 and 9 have been amended to improve grammar. Support for the claim amendments can be found in at least Figs. 1A-1B, 2A-2B, 3 and 4A-4B and Specification at paragraphs [0019]-[0023] and [0029]-[0034], among other places. Accordingly, no new matter has been added by the amendments.

### *Claim Rejections Under 35 U.S.C. § 102(b)*

Claims 2-4 and 15-20 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,694,257 ("Klein *et al.*," hereinafter, "Klein"). The Examiner takes the position that Klein discloses a semiconductor device including an integrated circuit buffer that receives an input signal and generates a plurality of output signals that relate to the input signal and an external resistor electrically connected to a delay generator, as well as other additional claimed features.

Withdrawal of the rejection of claims 2-4 and 15-20 is respectfully requested for at least the following reasons.

Present Invention

The present invention is directed to a semiconductor device having an integrated circuit buffer and a resistor. The buffer includes a delay generator. The buffer receives an input signal and generates a plurality of output signals that relate to the input signal. The delay generator is configured to phase-shift the timing of the plurality of output signals with respect to the input signal. The resistor has a resistance value, a first resistor end that is electrically

connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference. The resistor is external to the integrated circuit buffer, and the resistance value determines a magnitude of the phase-shift caused by the delay generator.

Klein

Klein discloses a circuit and method for demodulation of transmitted phase-coherent signal including recovery of the clock and data signals associated with the transmitted signal. The circuit includes a clock recovery circuit having a one-shot 12 having both inverting and non-inverting inputs for receiving the phase-coherent modulated signal. The circuit also includes a resistor 20, which is connected between the one-shot 12 and a source of supply voltage. The circuit also includes a capacitor 22 which is connected between the one-shot 12 and a ground reference. The one-shot 12 is coupled to an input of a divide-by-two circuit 14, the output of which is coupled to an input terminal of a multiplexer 16. The multiplexer 16, for receiving a transmitted clock signal on a second input terminal and for receiving an inverted silence signal, is coupled to a phase-locked loop (PLL) circuit 18. The phase-locked loop circuit 18 has an extracted clock output terminal, a two times clock output terminal and a four times clock output terminal. The one-shot 12 is used to recover the low frequency from the incoming signal. Every one-half bit time, another edge occurs which corresponds to the low frequency component. The output of the one-shot 12 is connected to the divide-by-two circuit 14 to obtain a square wave which is then fed to the phase-locked loop circuit 18 via the multiplexer 16. The multiplexer 16 is used to supply a frequency reference to the phase-locked loop circuit 18 and selects either the recovered clock signal or the transmitter clock signal (TXCLK) depending on whether there is in fact a valid signal being received. The data recovery circuit recovers the data by looking for an edge during a specific time window which is created using the extracted clock signal.

Claim 2

Claim 2, as amended, recites, *inter alia*:

> an integrated circuit buffer having a delay generator, the buffer receiving an input signal and generating a plurality of output signals that

> relate to the input signal, the delay generator being configured to phase-shift the timing of the plurality of output signals with respect to the input signal; and
>
> a resistor having a resistance value, a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference, the resistor being external to the integrated circuit buffer, the resistance value determining a magnitude of the phase-shift caused by the delay generator.

Klein fails to disclose or suggest a semiconductor that includes an integrated circuit buffer having a delay generator that is configured to phase-shift the timing of a plurality of output signals with respect to an input signal and a resistor which is external to the buffer and which has a resistance value that determines a magnitude of the phase-shift caused by the delay generator.

A claim is anticipated under 35 U.S.C. § 102 only if each and every element as set forth in the claim is found expressly or inherently described in a single prior art reference and the elements must be arranged as required in the claim. MPEP § 2131.

Klein discloses a circuit that demodulates a transmitted phase-coherent signal including recovery of clock and data signals. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals. Klein fails to disclose or even suggest phase-shifting an output signal with respect to an input signal by a magnitude that is determined by a resistance value of an external resistor.

It is therefore, respectfully submitted, that independent claim 2 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 2, as amended. Claims 3-4 depend from amended claim 2. Accordingly, Applicants respectfully request that the rejection of amended independent claim 2 and dependent claims 3-4 under 35 U.S.C. § 102(b) be withdrawn.

Claim 15

Claim 15, as amended, recites, *inter alia*:

> electrically connecting a first terminal of an external resistor to a buffer that generates a plurality of output signals, the external resistor having a resistance value and the buffer including a delay generator and a phase locked loop, the first terminal of the external resistor being electrically coupled to the delay generator;
>
> electrically connecting a second terminal of the external resistor to a ground or a voltage reference;
>
> receiving a clock input signal in the buffer; and
>
> phase-shifting the timing of one or more of the output signals with respect to the clock input signal in an amount that is dependent upon the resistance value of the external resistor.

Klein fails to disclose or suggest a method of adjusting the timing of an output signal of a semiconductor that includes connecting an external resistor to a buffer that generates a plurality of output signals and phase-shifting the timing of one or more of the output signals with respect to the clock input signal in an amount that is dependent upon a resistance value of the external resistor.

Klein discloses a circuit that demodulates a transmitted phase-coherent signal including recovery of clock and data signals. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals. Klein fails to disclose or even suggest phase-shifting the timing of one or more output signals with respect to a clock input signal in an amount that is dependent upon a resistance value of an external resistor.

It is therefore, respectfully submitted, that independent claim 15 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 15, as amended. Claim 16 depends from amended claim 15. Accordingly, Applicants respectfully request that the rejection of amended independent claim 15 and dependent claim 16 under 35 U.S.C. § 102(b) be withdrawn.

Claim 17

Claim 17, as amended, recites, *inter alia*:

> a buffer that receives the input signal from the input terminal and which is configured to generate a plurality of output signals and to phase-shift the timing of at least one of the plurality of output signals with respect to the input signal; and
>
> an external resistor coupled between the buffer and ground or a voltage reference, the external resistor having a resistance value that determines a magnitude of the phase-shift of the at least one of the plurality of output signals relative to the input signal.

Klein fails to disclose or suggest a semiconductor that includes a buffer configured to generate a plurality of output signals and to phase-shift the timing of at least one of the plurality of output signals with respect to the input signal and an external resistor having a resistance value that determines a magnitude of the phase-shift of the at least one of the plurality of output signals relative to the input signal.

Klein discloses a circuit that demodulates a transmitted phase-coherent signal including recovery of clock and data signals. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals. Klein fails to disclose or even suggest phase-shifting at least one of a plurality of output signals with respect to an input signal by a magnitude that is determined by a resistance value of an external resistor.

It is therefore, respectfully submitted, that independent claim 17 is not anticipated by Klein because Klein does not disclose or suggest each and every element of claim 17, as amended. Claims 18-20 depend from amended claim 17. Accordingly, Applicants respectfully request that the rejection of amended independent claim 17 and dependent claims 18-20 under 35 U.S.C. § 102(b) be withdrawn.

Claims 1 and 21

Claims 1 and 21 have been canceled, and therefore, the rejection of claims 1 and 21 under 35 U.S.C. § 102(b) has been effectively rendered moot.

***Claim Rejections under 35 U.S.C. § 103(a)***

Claims 6-7, 9-10 and 12-13 have bee rejected under 35 U.S.C. § 103(a) as being unpatentable over Klein in view of U.S. Patent No. 5,355,037 ("Andresen *et al.*," hereinafter, "Andresen"). The Examiner takes the position that Klein discloses all of the claimed limitations as recited in claim 1 (*sic.* – i.e., claim 2), but lacks a phased locked loop having a phase detector and a delay generator, a delay line and an external resistor that are electrically connected to adjust the timing. The Examiner takes the position that Andresen discloses a phased locked loop with a phase detector, a delay line and an internal feedback signal, and that it would have been obvious to modify the circuit of Klein to include the aforementioned features of Andresen.

Withdrawal of the rejection of claims 6-7, 9-10 and 12-13 is respectfully requested for at least the following reasons.

Andresen

Andresen discloses a phase-locked loop (PLL) circuit 10 which synchronizes a system clock signal with a chip clock signal of an individual integrated circuit. A system clock is input to a phase detector 11 and a delay path 13. The delay path 13 includes a digital delay line 15 and other delaying elements such as a high fanout clock distribution circuit 17. The clock distribution circuit 17 distributes the chip clock throughout the integrated circuit, and also feeds back the chip clock as an input to the phase detector 11. Because the system clock is provided at the input of delay path 13 and the chip clock is obtained at the output of delay path 13, the chip clock is time-shifted relative to the system clock due to the delay of the delay path 13.

Claims 6-7, 9-10 and 12-13

Claims 6-7, 9-10 and 12-13 depend upon independent claim 2, as amended.

In order to establish *prima facie* obviousness of a claimed invention, all the claimed limitations must be taught or suggested by the prior art. MPEP § 2143.03.

Klein fails to disclose, teach, or suggest a semiconductor that includes an integrated circuit buffer having a delay generator that is configured to phase-shift the timing of a

plurality of output signals with respect to an input signal and a resistor which is external to the buffer and which has a resistance value that determines a magnitude of the phase-shift caused by the delay generator. Klein discloses a circuit that demodulates a transmitted phase-coherent signal including recovery of clock and data signals, as required by all of claims 6-7, 9-10 and 12-13. The external resistor of Klein is used to adjust the time-delay of a one-shot which is applied to a divide-by-two circuit which in turn is applied to a phase-locked loop (PLL) by way of a multiplexer in order to demodulate the clock and data signals. Andresen fails to compensate for the deficiencies of Klein. Andresen merely discloses a phase-locked loop (PLL) circuit which synchronizes a system clock signal with a chip clock signal of an individual integrated circuit and a digital delay line.

Furthermore, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP § 2143.01. Modifying the data demodulation circuit of Klein by the phase-locked loop (PLL) circuit of Andresen will change the principle of operation of the Klein circuit and will likely result in a circuit that cannot demodulate data because the PLL of Andresen is expecting a clock signal not a data signal. The proposed combination suggested by the Examiner is a mere aggregation of components and would not result in a functioning device in accordance with the teachings of Klein or Andresen.

Thus, Klein modified by Andresen does not disclose all of the claimed features of claims 6-7, 9-10 and 12-13, as suggested by the Examiner. Therefore, claims 6-7, 9-10 and 12-13, are not *prima facie* obvious in view of Klein modified by Andresen. Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of claims 6-7, 9-10 and 12-13 should be withdrawn.

Claims 8, 11 and 14

Claims 8, 11 and 14 have been canceled, and therefore, the rejection of claims 8, 11 and 14 under 35 U.S.C. § 103(a) has been effectively rendered moot.

***Allowable Subject Matter***

The Examiner has stated that claim 5 is objected to as being dependent upon a rejected base claim but will be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Applicants have rewritten claim 5 in independent form including all the features of original base claim 2. Accordingly, the objection to claim 5 has been effectively overcome and should be withdrawn.

## CONCLUSION

In view of the foregoing Amendment and remarks , it is respectfully submitted that the present application, including claims 2-7, 9-10, 12-13 and 15-20, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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